Electronic Version
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Claims

[c1] 1. A pixel structure on a transparent substrate, the pixel structure comprising:
a scan line over the transparent substrate;
a gate insulation layer over the transparent substrate covering the scan line;
a data line over the gate insulation layer, wherein the data line extends in a direction perpendicular to the direction of extension of the scan line;
a shelling layer over the transparent substrate positioned on each side of the data line, wherein the shelling layers on each side of the data line are electrically connected;
a thin film transistor over the transparent substrate, wherein the thin film transistor has a gate electrode, a channel layer and a pair of source/drain terminals, the source terminal is electrically connected to the data line, the gate electrode is electrically connected to the scan line and the channel layer is formed over the gate insulation layer above the gate electrode;
a passivation layer over the transparent substrate covering the thin film transistor and the data line;
a contact within the passivation layer; and
a pixel electrode over the passivation layer, wherein the

pixel electrode is electrically connected to the drain terminal through the contact.

[c2] 2. The pixel structure of claim 1, wherein the shelling layer further includes:
a shelling section over the transparent substrate on each side of the data line; and
a connective section over the transparent substrate, wherein the connective section joins up the shelling section on each side of the data line electrically.

[c3] 3. The pixel structure of claim 1, wherein the shelling layer includes a block of shelling metallic layer that crosses from one side of the data line to the other.

[c4] 4. The pixel structure of claim 1, wherein the shelling layer, the gate electrode and the scan line are all fabricated using an identical material.

[c5] 5. A pixel structure on a transparent substrate, the pixel structure comprising:
a scan line over the transparent substrate;
a gate insulation layer over the transparent substrate covering the scan line;
a data line over the gate insulation layer, wherein the data line extends in a direction perpendicular to the direction of extension of the scan line;

a shelling layer over the transparent substrate on each side of the data line;
a dielectric layer between the data line and the gate insulation layer above the shelling layer;
a thin film transistor over the transparent substrate, wherein the thin film transistor has a gate electrode, a channel layer and a pair of source/drain terminals, wherein the source terminal is electrically connected to the data line, the gate electrode is electrically connected to the scan line and the channel layer is formed over the gate insulation layer above the gate electrode;
a passivation layer over the transparent substrate covering the thin film transistor and the data line;
a contact within the passivation layer; and
a pixel electrode over the transparent substrate, wherein the pixel electrode and the drain terminal are electrically connected through the contact.

[c6] 6. The pixel structure of claim 5, wherein the dielectric layer includes a silicon nitride layer.

[c7] 7. The pixel structure of claim 5, wherein the shelling layers on each side of the data line are electrically connected.

[c8] 8. The pixel structure of claim 7, wherein the shelling layer further includes:

a shelling section over the transparent substrate on each side of the data line; and

a connective section over the transparent substrate, wherein the connective section joins up the shelling section on each side of the data line electrically.

[c9] 9. The pixel structure of claim 8, wherein the shelling layer includes a block of shelling metallic layer that crosses from one side of the data line to the other.

[c10] 10. The pixel structure of claim 5, wherein the shelling layer, the gate electrode and the scan line are all fabricated using an identical material.

[c11] 11. A method of forming a pixel structure, comprising the steps of:

forming a gate electrode and a scan line having connection with the gate electrode over a transparent substrate and forming a shelling layer over the transparent substrate at the same time, wherein the shelling layer is formed on each side of an area destined to form a data line and the shelling layers on each side are electrically connected together;

forming a gate insulation layer over the transparent substrate covering the gate electrode, the scan line an the shelling layer;

forming a channel layer over the gate insulation layer

above the gate electrode;

forming a pair of source/drain terminals over the channel layer and forming a data line having connection with the source terminal over the gate insulation layer at the same time, wherein the gate electrode, the channel layer and the source/drain terminals together constitute a thin film transistor;

forming a passivation layer over the transparent substrate covering the thin film transistor and the data line;

forming an opening that exposes the drain terminal in the passivation layer; and

forming a pixel electrode over the passivation layer, wherein the pixel electrode and the drain terminal are electrically connected through a contact in the opening.

[c12] 12. The method of claim 11, wherein the shelling layer includes a shelling section on each side of the data line and a connective section joining the shelling sections electrically.

[c13] 13. The method of claim 11, wherein the shelling layer is a block of shelling metallic layer that crosses from one side of the data line to the other side.

[c14] 14. The method of claim 11, wherein the shelling layer, the gate electrode and the scan line are all fabricated using an identical material.

[c15] 15. A method of forming a pixel structure, comprising the steps of:

forming a gate electrode and a scan line having connection with the gate electrode over a transparent substrate and forming a shelling layer over the transparent substrate at the same time, wherein the shelling layer is formed on each side of an area destined to form a data line and the shelling layers on each side are electrically connected together;

forming a gate insulation layer over the transparent substrate covering the gate electrode, the scan line and the shelling layer;

forming a channel layer over the gate insulation layer above the gate electrode;

forming a dielectric layer over the gate insulation layer above the shelling layer;

forming a pair of source/drain terminals over the channel layer and forming a data line having connection with the source terminal over the gate insulation layer at the same time, wherein the gate electrode, the channel layer and the source/drain terminals together constitute a thin film transistor;

forming a passivation layer over the transparent substrate covering the thin film transistor and the data line;

forming an opening that exposes the drain terminal in

the passivation layer; and

forming a pixel electrode over the passivation layer, wherein the pixel electrode and the drain terminal are electrically connected through a contact in the opening.

[c16] 16. The method of claim 15, wherein the dielectric layer is a silicon nitride layer.

[c17] 17. The method of claim 15, wherein the shelling layers on each side of the data line are electrically connected together.

[c18] 18. The method of claim 17, wherein the shelling layer includes a shelling sections on each side of the data line and a connective section joining the shelling sections electrically.

[c19] 19. The method of claim 17, wherein the shelling layer is a block of shelling metallic layer that crosses from one side of the data line to the other side.

[c20] 20. The method of claim 15, wherein the shelling layer, the gate electrode and the scan line are all fabricated using an identical material.